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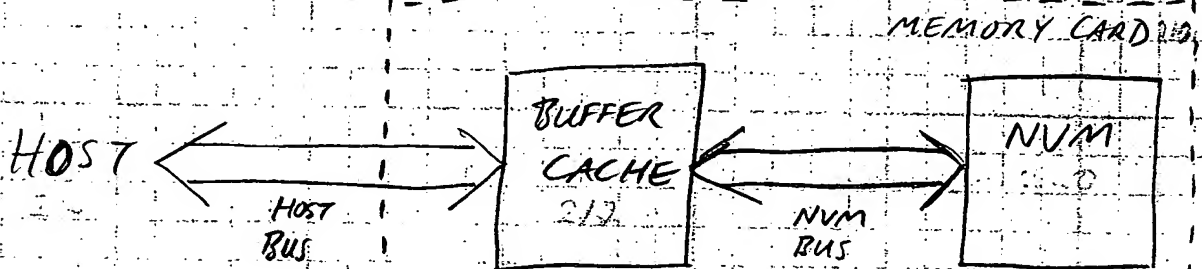


FIGURE 1 (PRIOR ART)

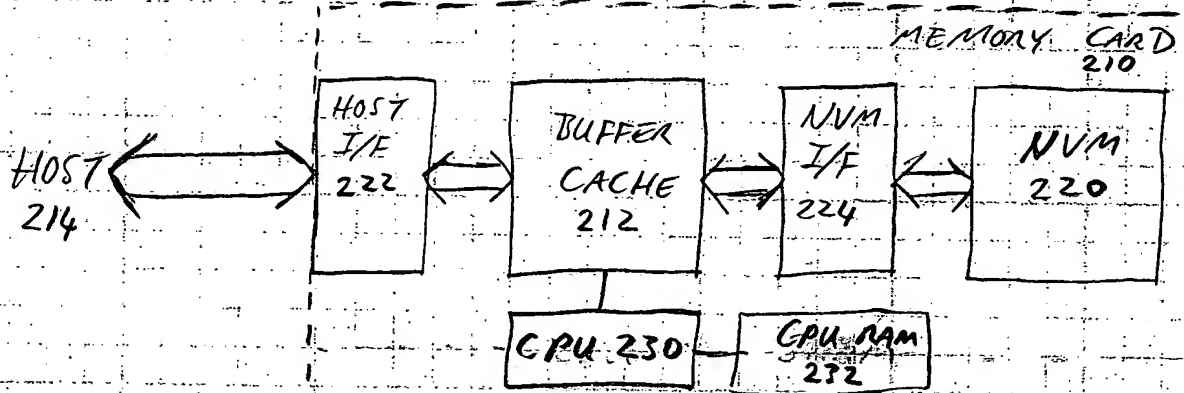


FIGURE 2

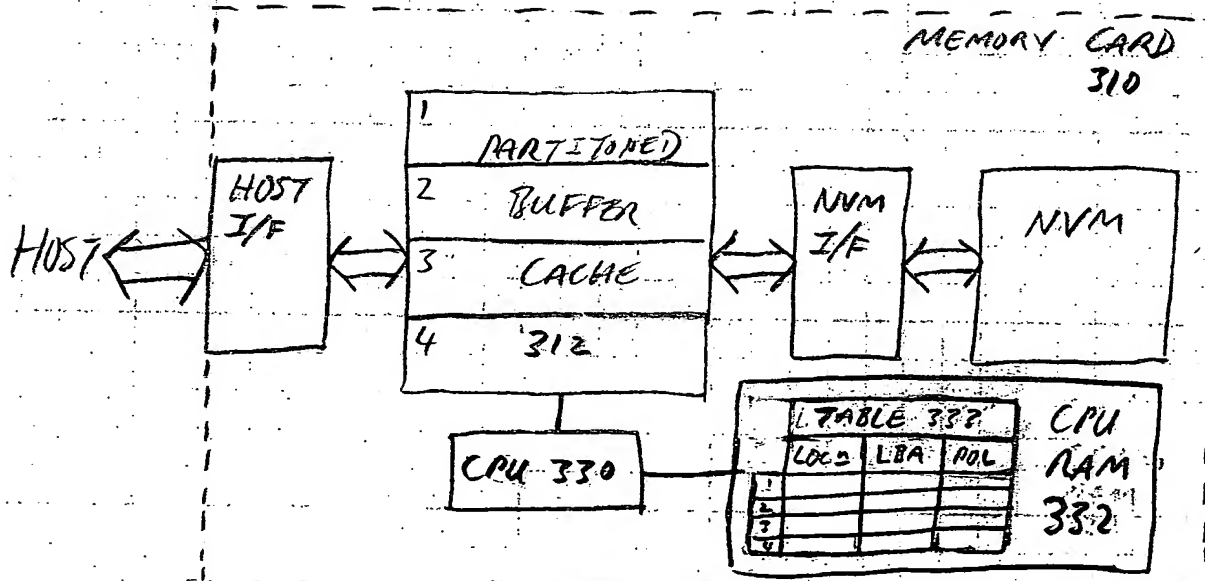


FIGURE 3

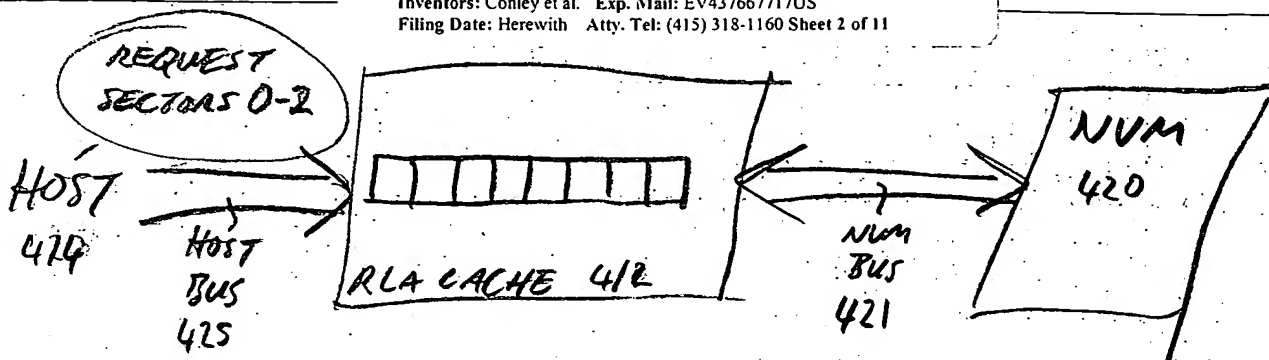


FIGURE 4A

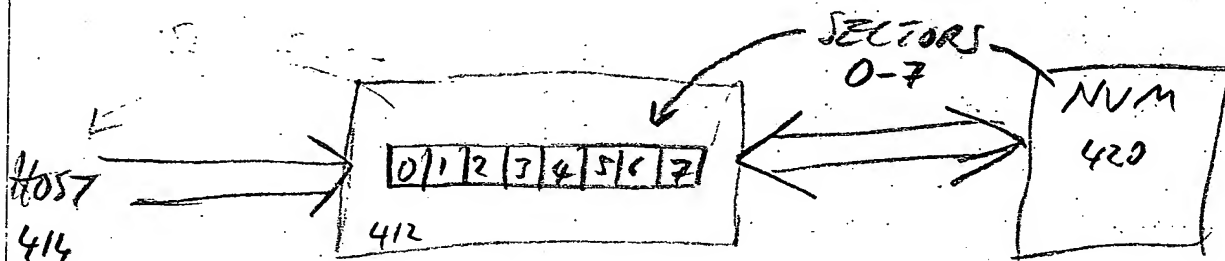


FIGURE 4B

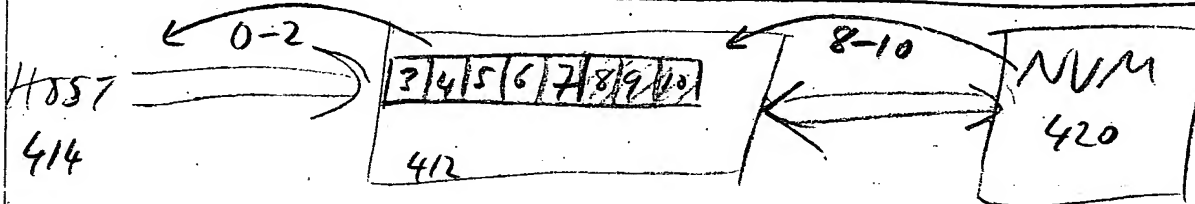


FIGURE 4C

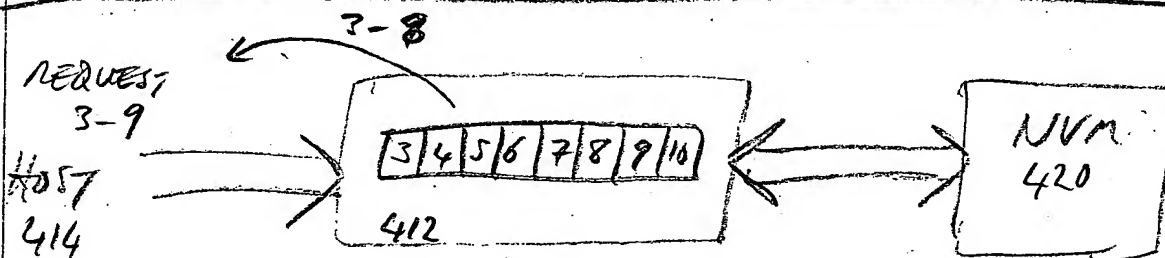


FIGURE 4D

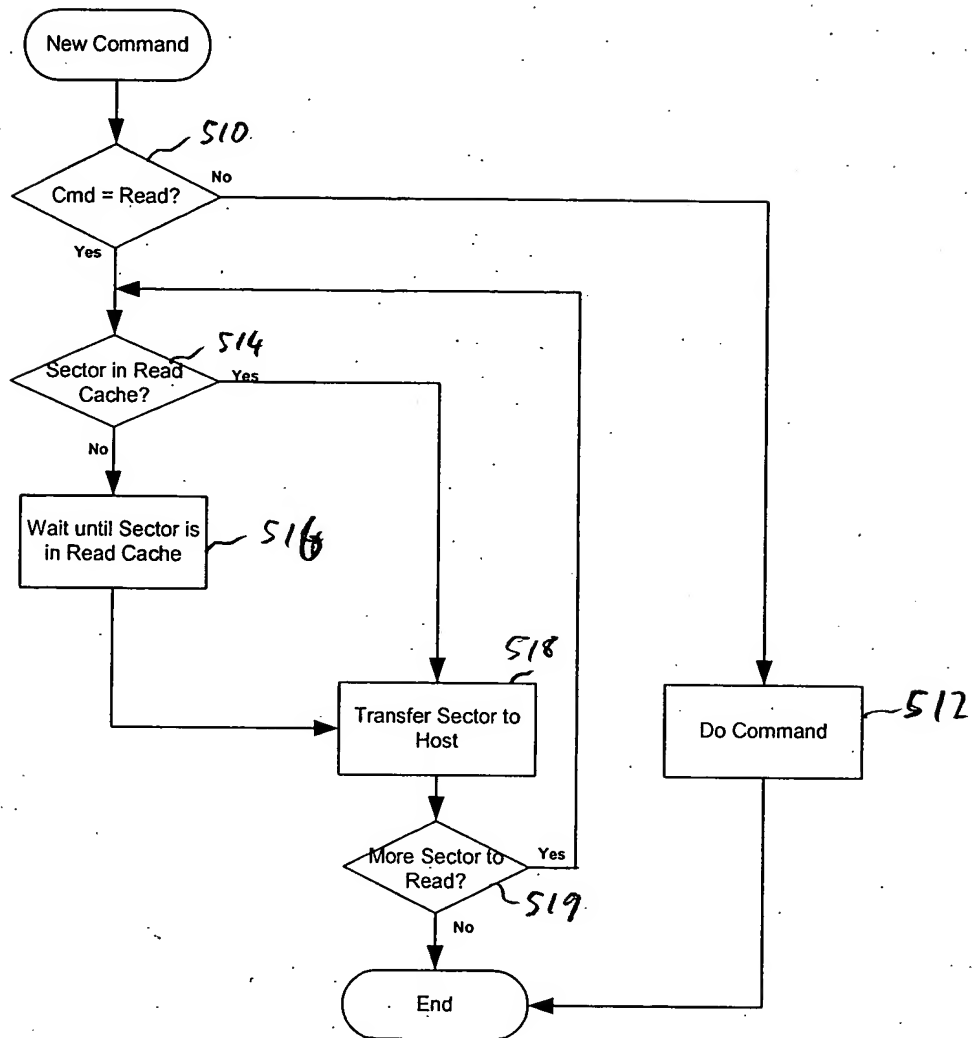


FIGURE 5 HOST COMMAND HANDLING PROCESS

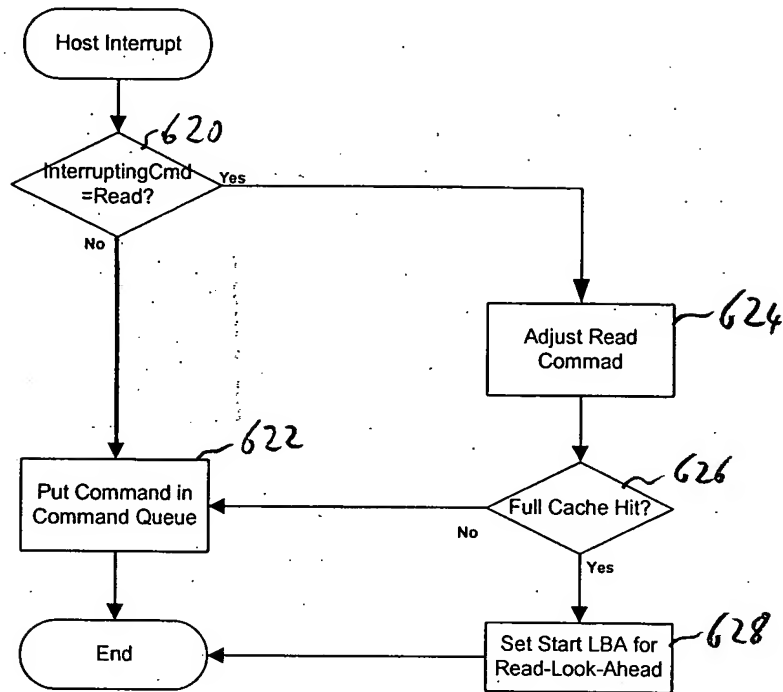


FIGURE 6A HOST INTERRUPT PROCESS

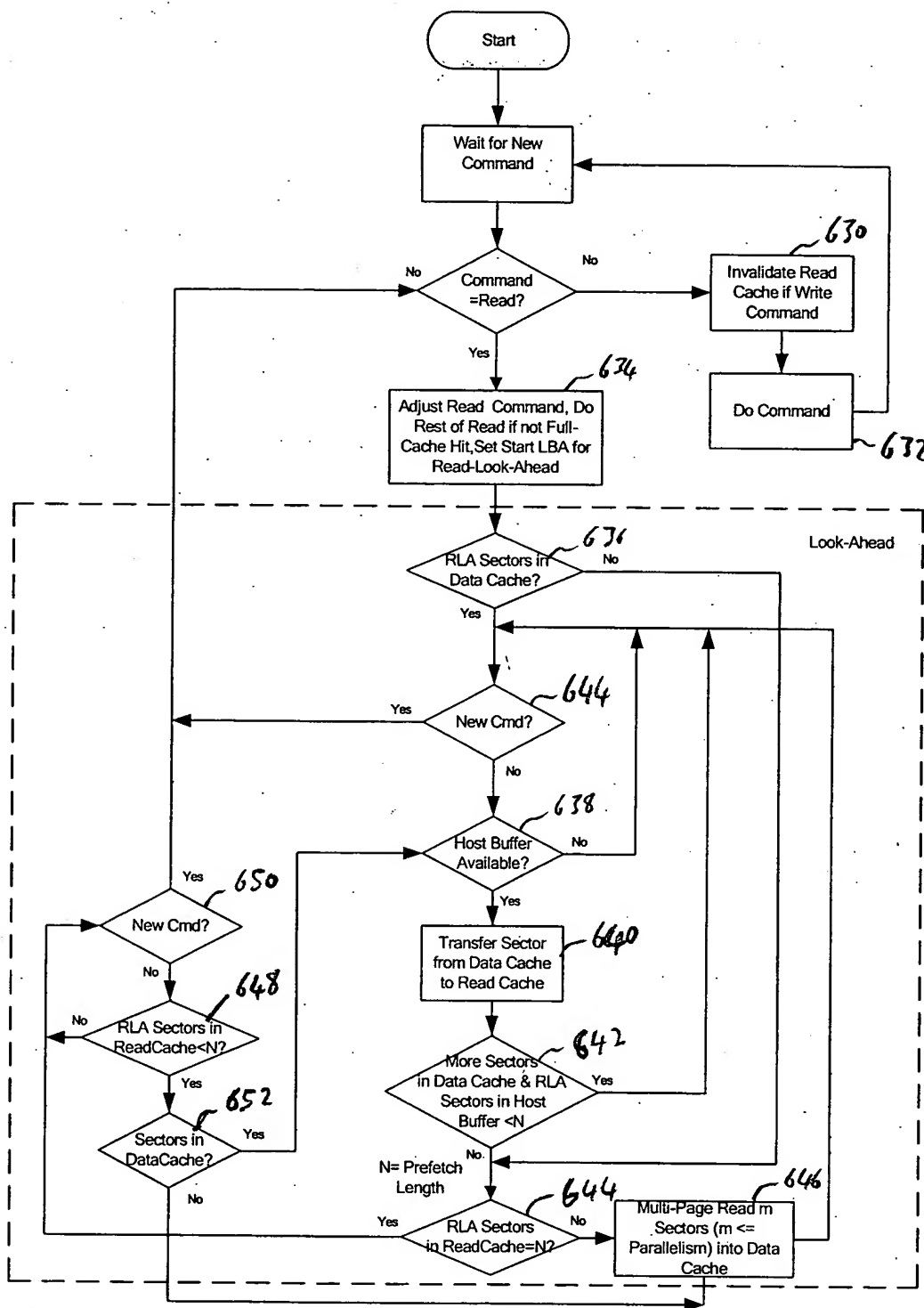


FIGURE 6B FLASH ACCESS MANAGEMENT PROCESS FLOW

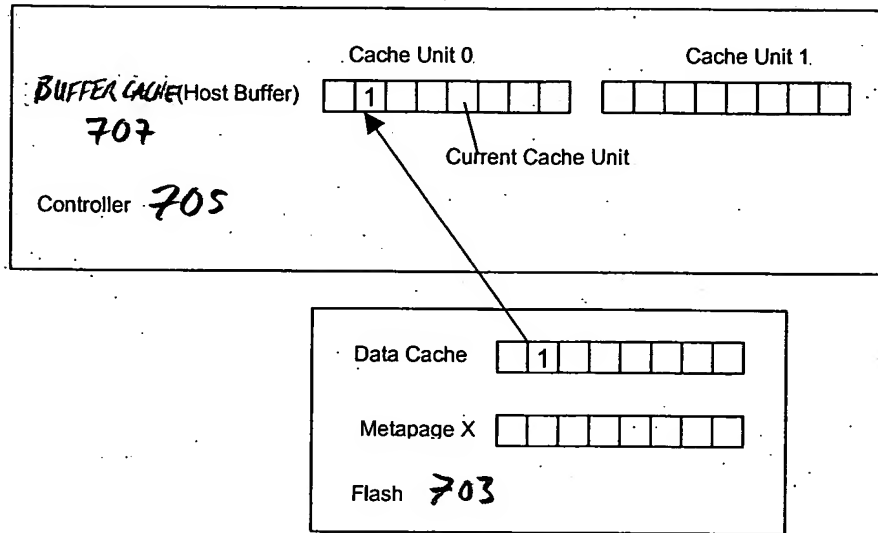


Figure 7 Cache configuration

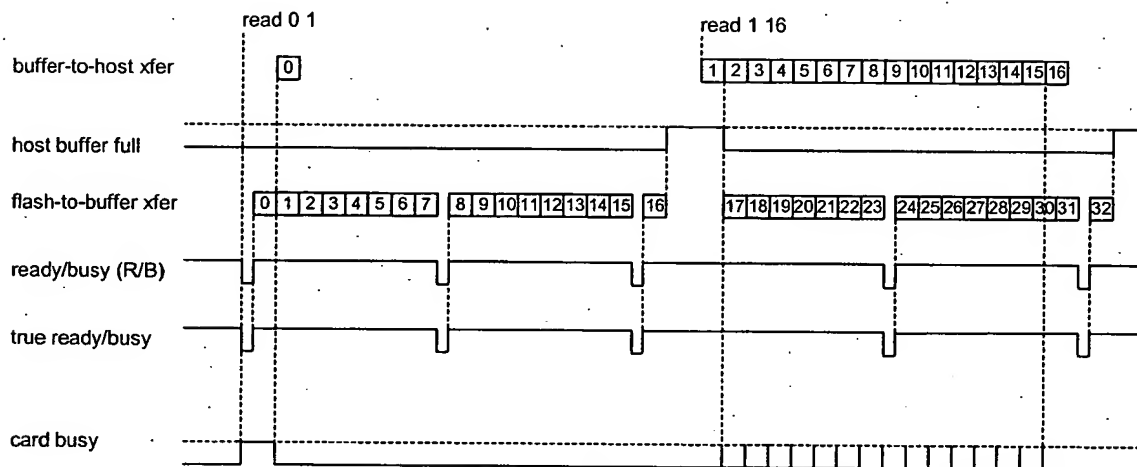


Figure 8A Cache hit

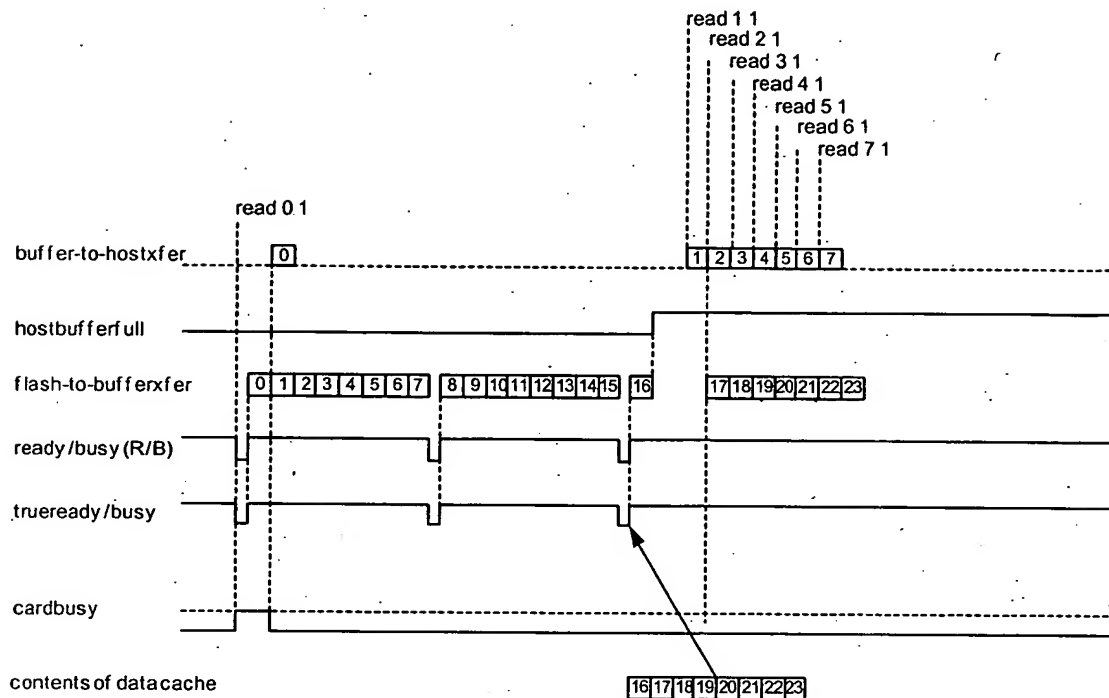


Figure 8B Cache hit

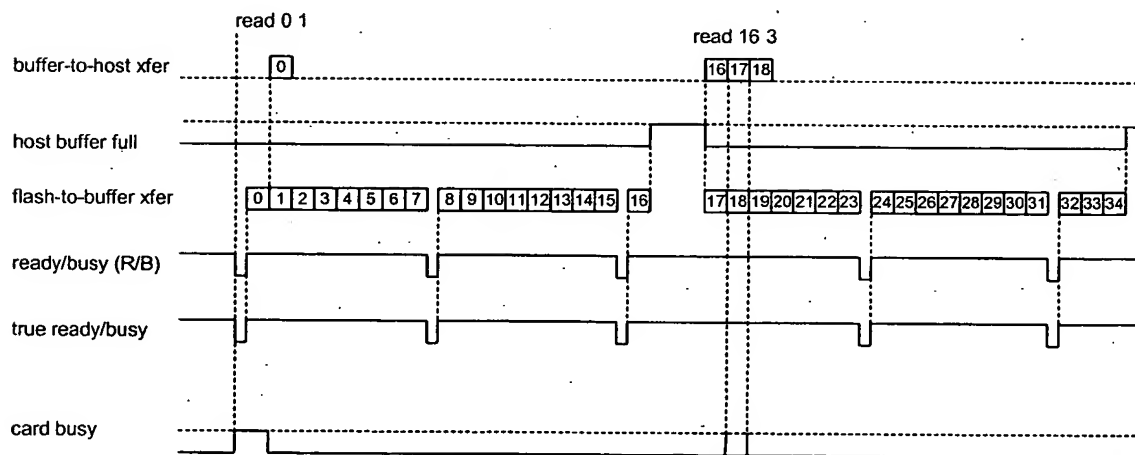


Figure 8C Partial hit

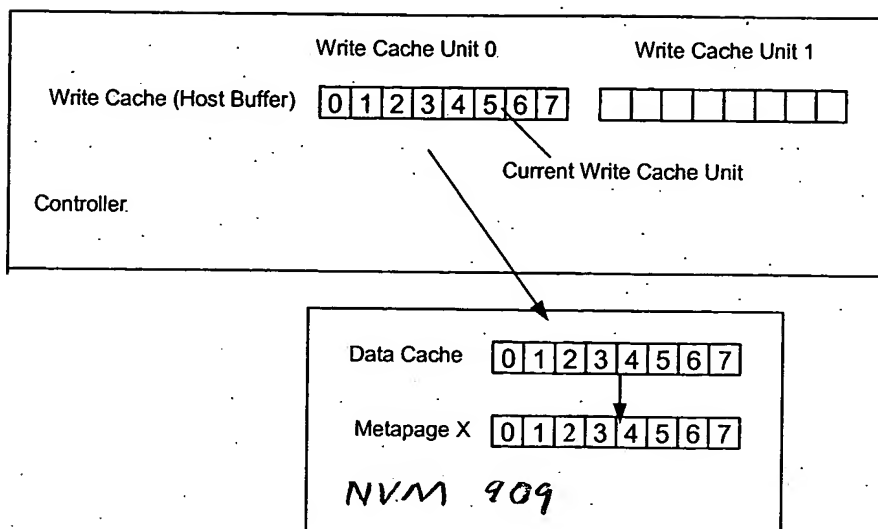


Figure 9

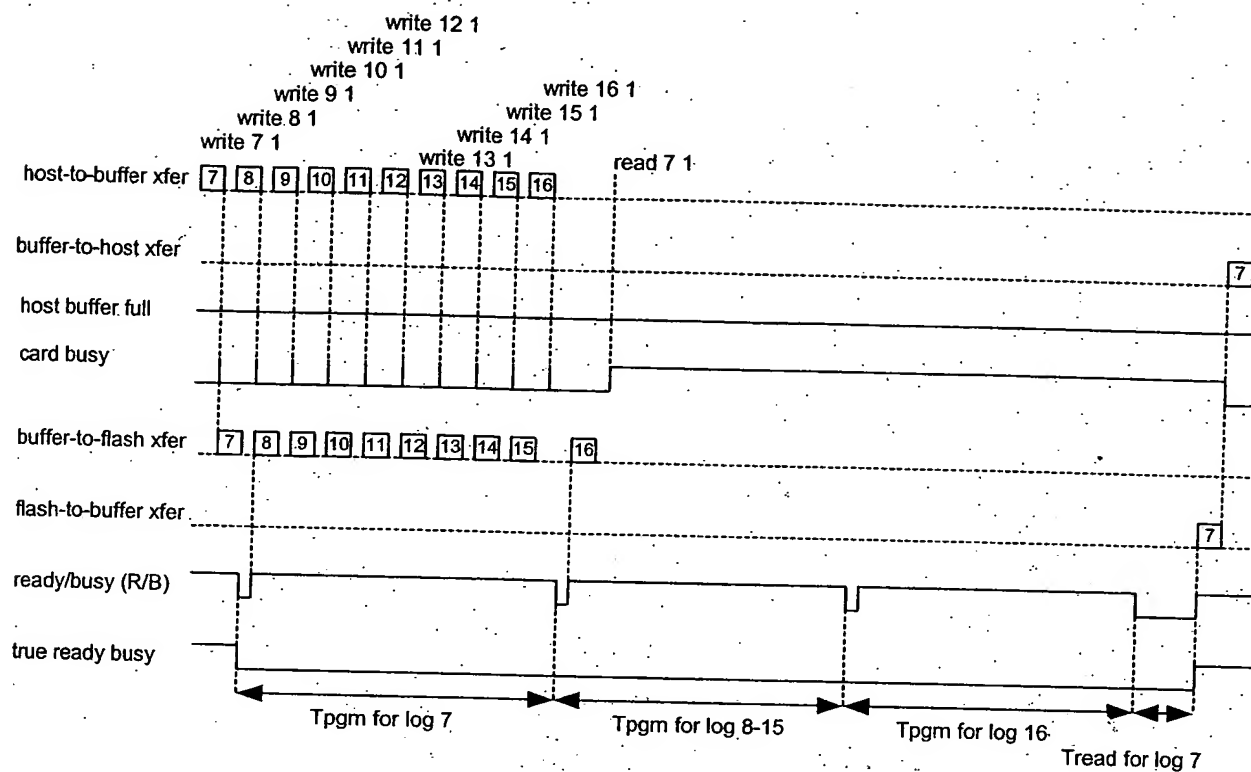
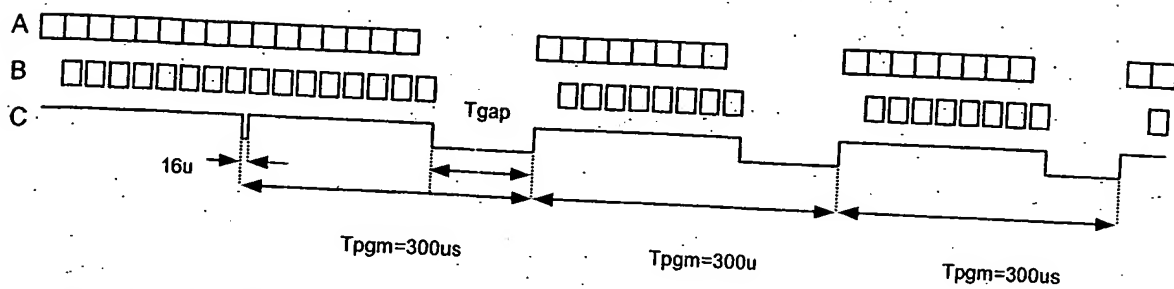


FIGURE 10



A= Host-to-Buffer Xfer, B= Buffer-to-Flash Xfer, C=Cache Busy(=R/B)

$T_{gap} = T_{xfer_flash} + T_{pgm} - (8 * T_{xfer_host})$

Flash command sequence= 80h11h...80h11h...80h15h72h

FIGURE 11

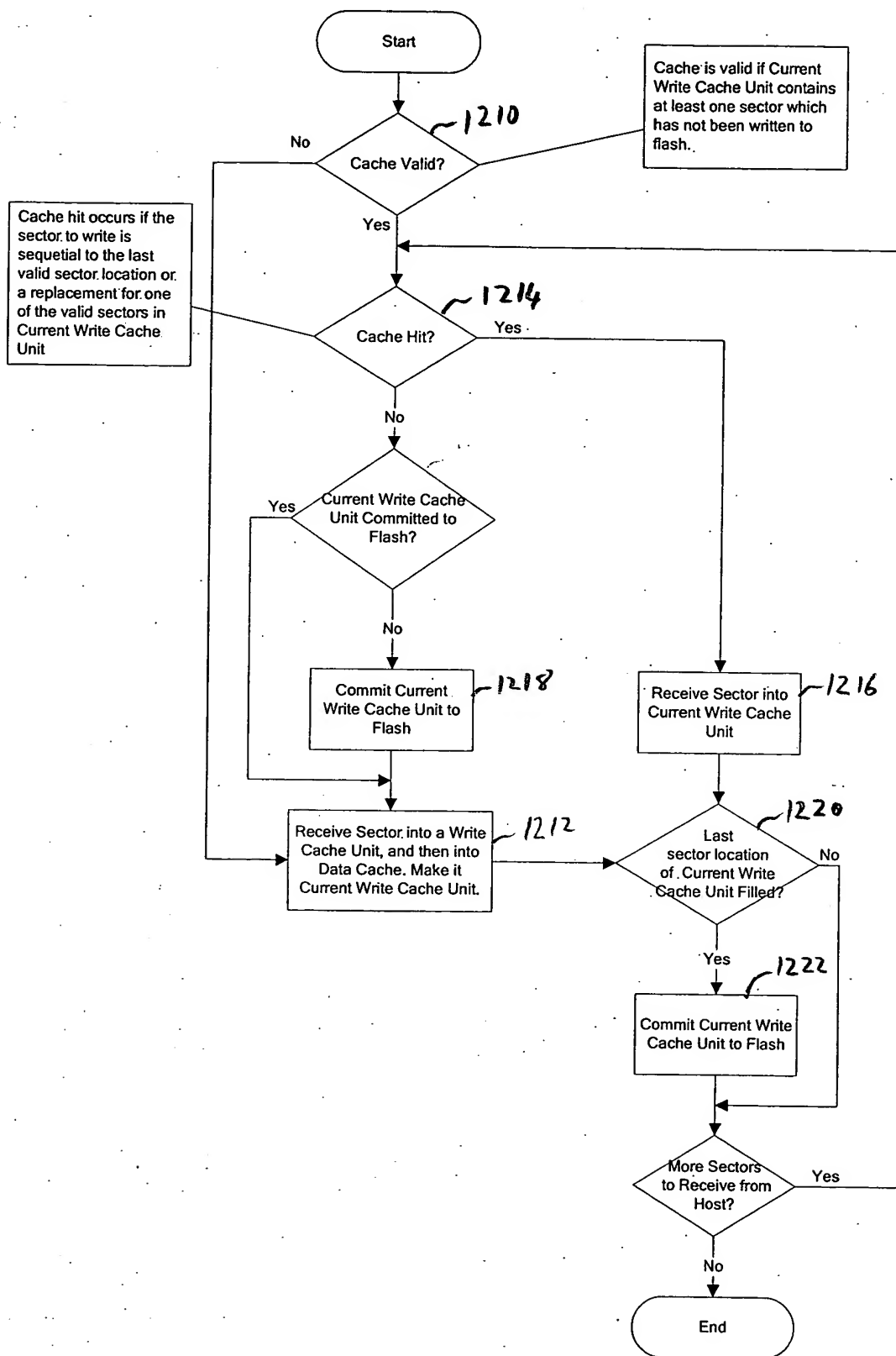


FIG. 12